Proceedings of the 2003 IEEE International Frequency Control Symposium and PDA Exhibition
Jointly with the 17th European Frequency and Time Forum

Optimized DRIE Etching of Ultra-Small Quartz Resonators

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Abstract – **Current manufacturing technology for quartz resonators does not provide a straightforward path for reducing the size and thereby increasing the frequency of operation into the UHF range. Using MEMS processing techniques and a commercial deep reactive ion etching (DRIE) tool, we are developing new techniques that may provide the ability to integrate large numbers of high performance filters onto a single chip for future handheld programmable communication systems.**
Keywords – **DRIE, quartz, resonators**

I. INTRODUCTION

Future wireless communication systems such as programmable radios and GPS receivers require ultra-small, high-Q, on-chip filters working in the VHF to UHF range [1]. To make such systems, one needs arrays of resonators that can be easily integrated with electronics. Until recently, most quartz manufacturers are making large, discreet devices using a wet etching process with either hydrofluoric acid or ammonium bifluoride [2]. The conventionally made quartz filters can not meet the requirements of those applications mentioned above. With the recent advancements in microfabrication technologies such as plasma etching and wafer bonding, we have developed a process for making miniaturized quartz resonators suitable for filter applications.

Our process relies on two dry plasma etches of AT-cut quartz in order to maintain precise geometrical control of sub-mm size quartz resonators. However, these two etching processes require somewhat different plasma conditions.

The first etch provides for thinning of an unpatterned quartz wafer that is bonded to a silicon handle wafer. This etch follows the initial lapping and polishing and must maintain a smooth surface finish (rms roughness < 1 nm) and should be as uniform as possible. The second etch occurs after the back-side metallization is deposited and defines the quartz resonator structures on the handle wafer. For this etch, the resonators are masked and sidewall control and low mask erosion are important. We have found that even for a reduced power condition (compared to the quartz thinning etch), resist masks can overheat and can be hardened. Moreover, the resist-to-quartz etch rate ratio can be as high as 1.5/1 for high bias conditions. This requires the use ultra-thick resists for adequate masking. We have therefore been developing quartz etching parameters that provide for higher mask selectivity, good sidewall control, and low resist heating for this second etch. Design of experiment (DOE) techniques have been utilized to determine an optimal set of etch and passivation gas parameters that provide for high spatial resolution for quartz-based MEMS devices. We will describe the results of these experiments in this paper.

II. PROCESS FLOW FOR RESONATOR

The quartz resonator fabrication process is illustrated in figure 1. Two of the key processing steps involve the deep reactive ion etching (DRIE) of quartz wafers using a Unaxis SLR inductively-coupled plasma (ICP) etcher. The starting materials for this process are an AT-cut single crystal quartz wafer, a <100>-oriented, n-type, 1-10 ohm-cm, silicon handle wafer, and a high-resistivity III-V compound semiconductor such as a GaAs wafer or a silicon-germanium substrate. The process begins with etching a small cavity into the silicon handle wafer to later accommodate the top metal electrodes of the quartz wafer. The quartz wafer is metallized with the aforementioned electrodes and then aligned and bonded with EV Group's EV-620 aligner and EV-501 bonder. The bonded quartz is subsequently thinned to a thickness of approximately 25 μm using conventional lapping and polishing techniques. Its thickness is further reduced to less than 10 μm using an SF_6-based plasma etch in the Unaxis etcher. The plasma thinning of quartz will be discussed in detail in a later section.

Once the quartz wafer is thinned to its final thickness, the bottom side metal electrodes can be deposited onto it. The continuous sheet of quartz is then patterned and etched using a thick photoresist mask and a CF_4-based plasma in the Unaxis tool to delineate the resonator patterns. Both the thick resist and CF_4-based plasma etch will be discussed later in detail.

For the III-V substrate, it is first patterned and etched to create protrusions on its surface using a citric acid-based etchant. Then, metals are deposited to form the bond pads for the subsequent thermal compression bond. In this bonding step, the Si/quartz pair is first aligned to the III-V substrate using EV Group's EV-620 aligner and then bonded at 350°C in the EV-501 wafer bonder. Finally, the silicon handle wafer is removed using either a dry or wet etching process to leave the completed quartz on the III-V substrate.

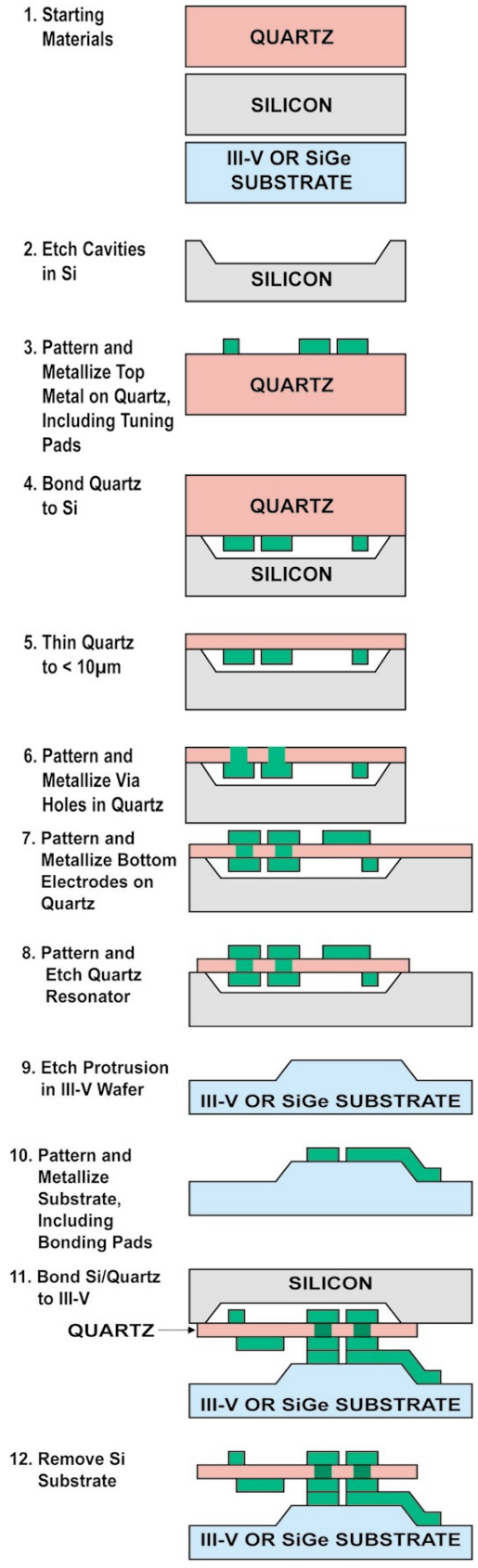

Fig. 1. Quartz resonator fabrication process flow.

III. SF_6-BASED DRIE THINNING OF QUARTZ

The plasma quartz thinning was performed in a Unaxis SLR deep reactive ion etcher (DRIE). This system has both an RIE unit similar to a parallel plate plasma etcher and an additional inductively-coupled plasma (ICP) coil that generates the plasma above the RIE. The advantage of using such a system is that it allows the creation of a high density plasma without using very high RIE power. Thus, DRIE offers a very fast etch rate without causing too much plasma damage to the etched substrates.

Thinning the quartz wafer requires using a higher plasma bias voltage and a higher RIE power than what is customary for traditional DRIE silicon etching. In addition, no passivation gas is needed for controlling the sidewall profile. Using 45 sccm of SF_6 and 10 sccm of argon at a pressure of 10mT, we applied 200 W of RIE power and 800 W of ICP power. These plasma conditions yielded a substrate bias voltage of -360 V, and we obtained a final surface roughness of 0.24 nm (rms) after removing 22 µm of material with an etch rate of 0.22 µm/min. The surface roughness measurement was performed using a Veeco optical profilometer. This level of roughness is comparable to the best surface quality obtainable for high grade quartz.

IV. THICK RESIST PROCESS

Once the quartz is thinned down to the desired thickness, we need to pattern the individual resonators by etching through the quartz layer using a mask. Most of the researchers doing patterned quartz dry etching are using a hard metal mask [3]. A typical process involves dry etching the quartz with a nickel mask and then metallizing the surface with a shadow mask. This technique works well for very large feature size. However, for our resonators, which have lateral dimensions on the order of 10's of microns, removing the hard mask and re-depositing metal electrodes to precise locations prove to be difficult. Therefore, we decided to fabricate all electrodes on the quartz wafer prior to defining the resonators with a removable, soft photoresist mask. The resist we chose was the Shipley SJR-5740 positive photoresist. When spun at 500 rpm and baked at 110°C for 15 minutes, the resist gives a thickness of 50 microns per layer. Figure 2 shows the SEM photo of the ultra-thick resist.

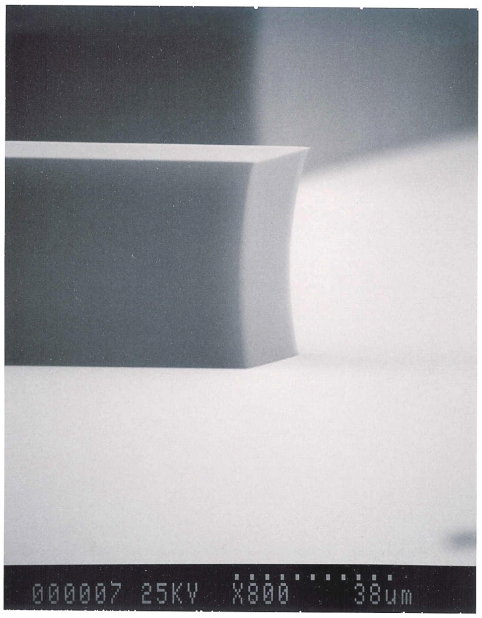

Fig. 2. 50-micron-thick Shipley SJR-5740 photoresist exposed with 1800 mJ/cm2 dose.

V. CF_4-BASED DRIE PATTERNING OF QUARTZ

Our initial attempt to pattern quartz was to use the SF_6-based quartz thinning recipe developed in section III with the thick resist process. The result was unsatisfactory. Major surface roughness appeared in the etched area due to the sputtering of resist mask because of high self-bias voltage of –360 V. In addition, the high self-bias voltage caused a very high resist erosion rate (Figure 3). The resist layer also became carbonized and could not be stripped easily. It became clear that a modified recipe with a significantly reduced self-bias voltage was needed to perform this task.

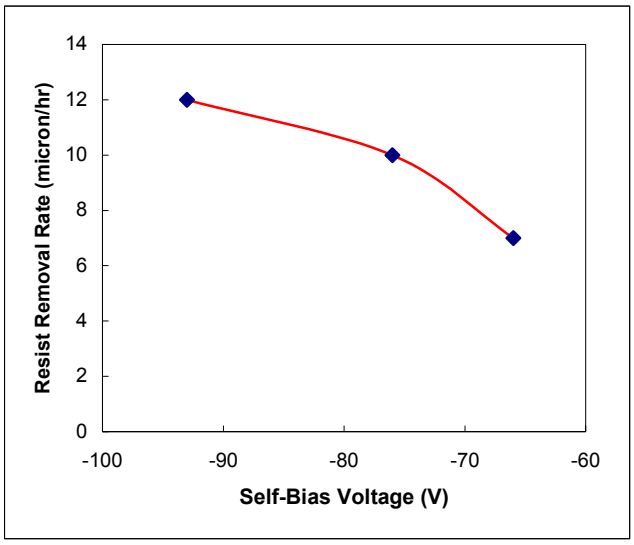

Fig. 3. Shipley SJR-5740 resist erosion rate vs. self-bias voltage

It was determined experimentally that for a given set of power and gas flow parameters, the chamber pressure has the strongest influence on the self-bias voltage. Furthermore, a lower chamber pressure produces a less negative self-bias voltage, which in turn gives a lower resist removal rate. Figure 4 shows the bias-voltage vs. pressure plot. The optimal etch recipe was determined to be 20 sccm of CF_4, 2 sccm of O_2 at a pressure of 2mT with 900 W of ICP power and 25 W of RIE power. The resulting self-bias voltage was –78V. We switched from SF_6 to CF_4 because the CF_4-based chemistry tends to produce a more vertical sidewall profile due to its passivating nature.

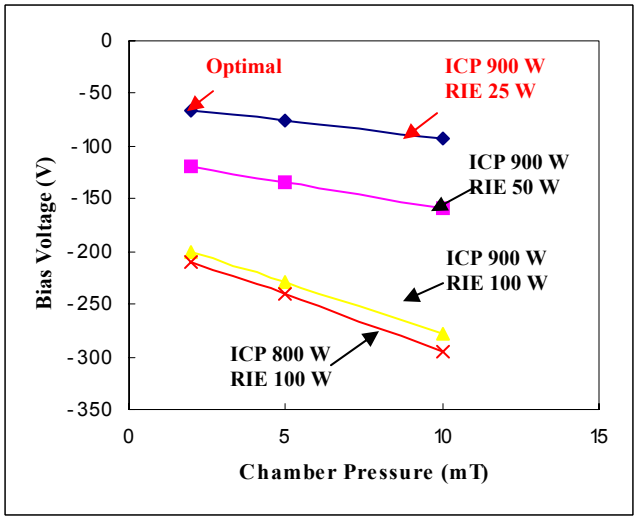

Fig. 4. Self-Bias Voltage vs. Chamber Pressure for various ICP and RIE power levels.

We then applied this optimized recipe to an AT-cut quartz wafer with a Shipley SJR-5740 resist coating. The wafer was etched for 2 hours in the Unaxis etcher (Figure 5). We obtained a quartz etch rate of 6 microns per hour and a resist erosion of 7 microns per hour for a nearly 1:1 quartz to resist etch selectivity. There was no micro-masking and grassing in the field due to re-deposition of the photoresist. Furthermore, the photoresist mask did not become carbonized and reticulated.

The photoresist was then completely removed from the patterned AT-cut quartz using a combination of an oxygen plasma ashing treatment (200mT, 200 W, 5 min) and a wet strip step with J. T. Baker's PRS-1000 photoresist stripper at 100 degrees C for 30 minutes. Figure 6 shows that both the etched and unetched surfaces remain smooth after the etch and resist strip. The previously masked area was clean and free of photoresist residues.

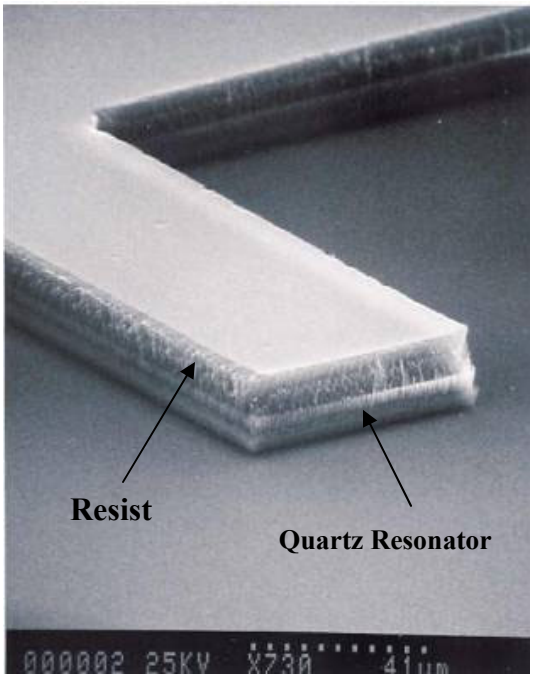

Fig. 5. SEM photograph of an etched, 12-micron-tall quartz structure with the photoresist mask.

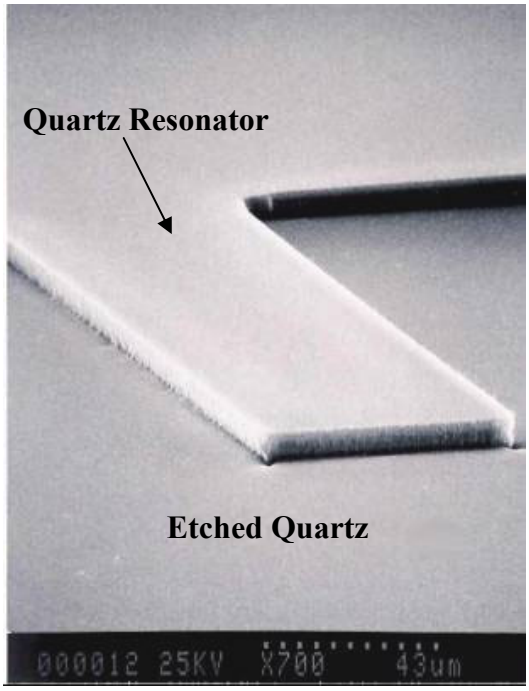

Fig. 6. SEM photograph of an etched, 12-micron-tall quartz structure with the photoresist mask completely removed.

We are currently fabricating the quartz resonators using the plasma thinning and patterning processes described above. The complete fabrication and performance evaluation results will be prepared in a later publication.

VI. CONCLUSION

Two deep reactive ion etching processes have been developed to miniaturize quartz resonators for wireless communication applications. The first one uses an SF_6-based chemistry with high bias voltage for high-rate thinning of quartz while maintaining mirror-like surface smoothness. The second process makes use of the CF_4-based chemistry to produce high-aspect- ratio, micron-size quartz structures. Both processes will be used to make ultra-small, integrated UHF quartz filters possible.

ACKNOWLEDGMENT

The authors would like to thank Dr. John Vig for his valuable technical discussions and support. This project is being funded by DARPA's Microsystems Technology Office under contract DAAB07-02-C-P613.

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